

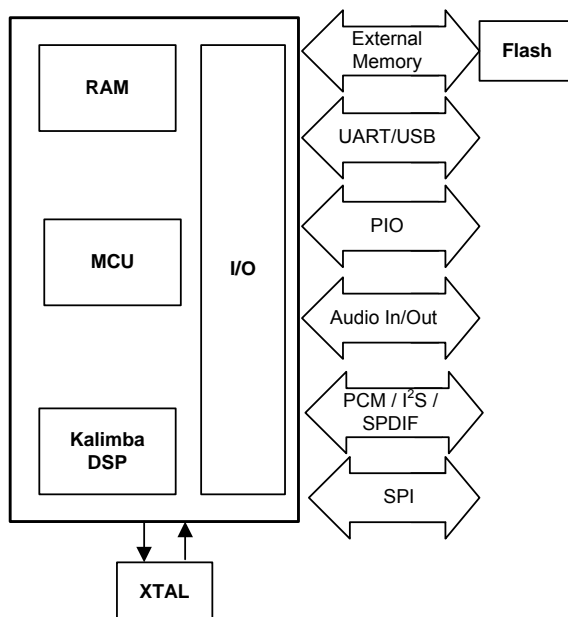
Features

- RISC Co-processor
- Kalimba DSP Co-processor
- Very High Quality 16-bit Internal Stereo CODEC
- Minimum External Components
- Low-Power 1.5V Operation, 1.8V to 3.6V I/O
- Integrated 1.5V and 1.8V Linear Regulators
- Integrated Switched-Mode Regulator
- Integrated Battery Charger
- USB and Dual UART Ports to 4Mbits/s
- Ability to Access up to 32Mbits of External Flash Memory (8Mbits Typical)
- I²S and SPDIF Interfaces
- Enhanced Audibility and Noise Cancellation
- 8mm x 8mm x 1.2mm TFBGA
- RoHS Compliant

Description

The Multimedia Applications Processor (MAP) is a single chip that provides multimedia applications for VoWiFi phone solutions and internet radio.

MAP interfaces up to 32Mbit of external flash memory. When used with CSR UniFi-1, it provides a complete solution for a VoWiFi phone or internet radio.



MAP System Architecture

Multimedia Application Processor

Single Chip for Multimedia Applications

Advance Information Product Brief for

BC57E687A

February 2007

www.csr.com

Applications

- VoWiFi phones
- Internet radio

MAP contains the Kalimba DSP co-processor, allowing for support of enhanced audio applications.

MAP has been designed to reduce the number of external components required which ensures production costs are minimised.

Key Features

Input Clock Support

- Crystal oscillator with built-in digital trimming
- Compatible with crystals between 8MHz and 32MHz (in multiples of 250kHz) or an external clock
- Accepts 7.68, 14.44, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz TCXO frequencies for GSM and CDMA devices with sinusoidal or logic level signals

Physical Interfaces

- Synchronous serial interface up to 4M data rate
- Optional I²C compatible interface
- UART interface with programmable data rate up to 3M data rate with an optional bypass mode
- Full-speed USB v1.1 interface
- Bi-directional serial programmable audio interface supporting PCM, I²S and SPDIF formats
- Two LED drivers with faders

Stereo Audio CODEC

- Very high quality internal stereo CODEC
- Dual ADC and DAC for stereo audio
- Integrated amplifiers for driving 16Ω speakers; no need for external components
- Integrated low-noise microphone bias
- 16-bit resolution, standard sample rates of 8kHz, 11.025kHz, 16kHz, 22.05kHz, 32kHz, 44.1kHz and 48kHz (DAC only)

RISC Co-Processor

- External flash extendable to 32Mbit
- Internal 48Kbyte RAM

Kalimba DSP

- Very low power Kalimba DSP co-processor, 64MIPs, 24-bit fixed point core
- Approximately 60mW power consumption when streaming music
- Single-cycle MAC; 24 x 24-bit multiply and 56-bit accumulator
- 32-bit instruction word, dual 24-bit data memory
- 24Kbyte (6Kword) program RAM, 36Kbyte + 48Kbyte (16Kword + 12Kword) data RAM
- 64words x 32-bit program memory cache when executing from flash

Auxiliary Features

- Power management includes digital shut-down and wake-up commands with an integrated low-power oscillator for ultra-low power
- On-chip regulators: 1.5V output from 1.8V to 2.7V input and 1.8V output from 2.7V to 4.5V input
- On-chip high-efficiency switched-mode regulator; 1.8V output from 2.7V to 4.4V input
- Power-on-reset cell detects low supply voltage
- 10-bit ADC and 8-bit DAC available to applications
- On-chip charger for lithium ion/polymer batteries

Package Options

- TFBGA, 8mm x 8mm x 1.2mm, 0.5mm pitch

Ordering Information

Interface Version	Package			Order Number
UART and USB	Type	Size	Shipment Method	BC57E687A-ITB-E4 ⁽¹⁾
	TFBGA (Pb free)	8mm x 8mm x 1.2mm 0.5 pitch	Tape and reel	

⁽¹⁾ Until BC57E687A reaches Production status order number is BC57E687A-ES-ITB-E4.

Minimum Order Engineering Sample Quantity: 2kpcs taped and reeled

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Document History

Revision	Date	History
1	20 NOV 06	Original publication of this document. (CSR reference: CS-110556-PBP)
2	11 DEC 06	Amended Key Features
3	06 FEB 07	Updated Applications

Multimedia Applications Processor

Product Brief

CS-110556-PBP3

February 2007